MOTOROLA

SEMICONDUCTORS

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC145104
MC145106
MC145107
MC145109
MC145112

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

PLL FREQUENCY SYNTHESIZERS

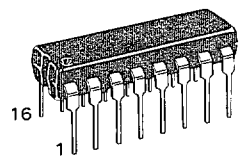
PLL FREQUENCY SYNTHESIZERS

The MC145104, MC145106, MC145107, MC145109, and MC145112 are phase locked loop (PLL) frequency synthesizer parts constructed with CMOS devices on a single monolithic structure. These synthesizers find applications in such areas as CB and FM transceivers. The device contains an oscillator/amplifier, a 2^{10} or 2^{11} divider chain for that oscillator signal, a programmable divider chain for the input signal and a phase detector. The MC145104/5106/5112 have circuitry for a 10.24 MHz oscillator or may operate with an external signal. The MC145107/5109 require the external reference signal. Several of the circuits provide a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 (MC145106/5109/5112) or 2^8 (MC145104/5107) programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground-to-supply binary signals. Pull-down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

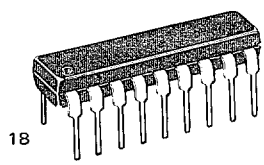
The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out of lock signal is provided from the on-chip lock detector with a "0" level for the out of lock condition.

The MC145106 is the full pinout version of this family of parts and has the capability of all parts in the family. The MC145104/5107/5109/5112 are limited pinout versions. See block diagrams for details.

- Single Power Supply
- Wide Supply Range: 4.5 to 12 Vdc
- 16 or 18 Pin Plastic Packages
- 10.24 MHz Oscillator on Chip
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On-Chip Pull Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11}



P SUFFIX
PLASTIC PACKAGE
CASE 648



P SUFFIX
PLASTIC PACKAGE
CASE 707

Pin-for- Pin Replacements for:
MC145104 for SM5104, MM55104, MM55114
MC145106 for MM55106, MM55116
MC145107 for SM5107
MC145109 for SM5109
MC145112 for SM5106

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to + 12	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out} \leq V_{DD}$.

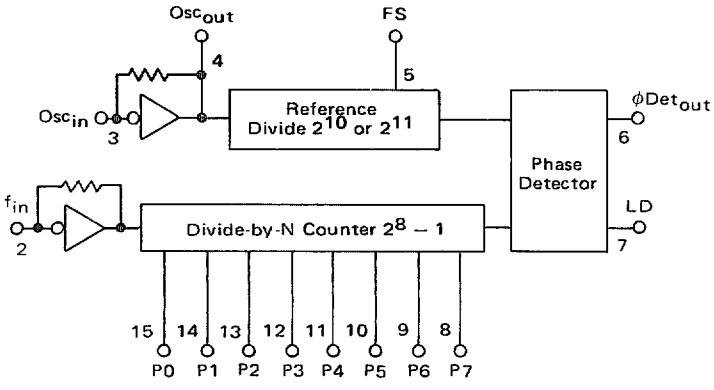
DS9515
Replaces ADI-431

RECOMMENDED OPERATION: DC Supply Voltage 4.5 to 12 Vdc

ELECTRICAL CHARACTERISTICS (T_A = 25° unless otherwise stated.)

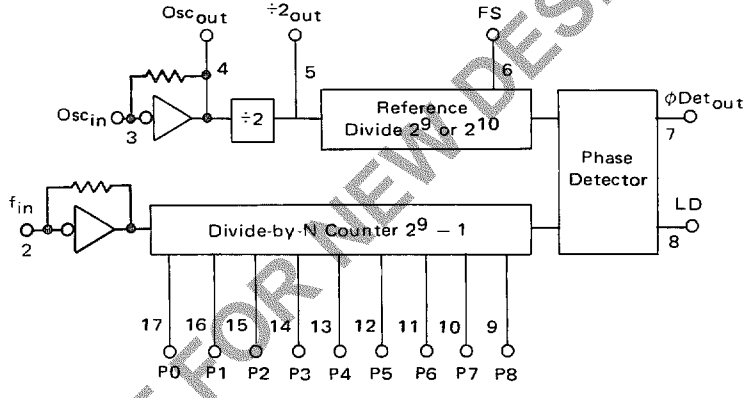
Characteristic		Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Supply Current		I_D	5.0	–	6	10	mAdc
			10	–	20	35	
			12	–	28	50	
Input Voltage	"0" Level	V_{IL}	5.0	–	–	1.5	Vdc
			10	–	–	3.0	
			12	–	–	3.6	
	"1" Level	V_{IH}	5.0	3.5	–	–	Vdc
			10	7.0	–	–	
			12	8.4	–	–	
Input Current (FS) (Pull-up Resistor)	"0" Level	I_{in}	5.0	-5.0	-20	-50	μAdc
			10	-15	-60	-150	
			12	-20	-80	-200	
(P0 to P8)			5.0	–	–	-0.3	
			10	–	–	-0.3	
			12	–	–	-0.3	
(FS)	"1" Level		5.0	–	–	0.3	μAdc
			10	–	–	0.3	
			12	–	–	0.3	
(P0 to P8) (Pull-down Resistor)			5.0	7.5	30	75	
			10	22.5	90	225	
			12	30	120	300	
(Osc_{in}, f_{in})	"0" Level		5.0	-2.0	-6.0	-15	μAdc
			10	-6.0	-25	-62	
			12	-9.0	-37	-92	
(Osc_{in}, f_{in})	"1" Level		5.0	2.0	6.0	15	
			10	6.0	25	62	
			12	9.0	37	92	
Output Drive Current		I_{OH}					mAdc
(V_O = 4.5 Vdc)	Source		5.0	-0.7	-1.4	–	
(V_O = 9.5 Vdc)			10	-1.1	-2.2	–	
(V_O = 11.5 Vdc)			12	-1.5	-3.0	–	
(V_O = 0.5 Vdc)	Sink	I_{OL}	5.0	0.9	1.8	–	mAdc
(V_O = 0.5 Vdc)			10	1.4	2.8	–	
(V_O = 0.5 Vdc)			12	2.0	4.0	–	
Input Amplitude		–					Vp-p
(f_{in} @ 4.0 MHz)			–	1.0	0.2	–	Sine
(Osc_{in} @ 10.24 MHz)			–	1.5	0.3		
Input Resistance		R_{in}					MΩ
(Osc_{in}, f_{in})			5.0	–	1.0	–	
			10	–	0.5	–	
			12	–	–	–	
Input Capacitance (Osc_{in}, f_{in})		C_{in}	–	–	6.0		pF
Three State Leakage Current (ϕ Det_{out})		I_{TL}					μAdc
			5.0	–	–	1.0	
			10	–	–	1.0	
			12	–	–	1.0	
Input Frequency (-40°C to +85°C)		f_{in}	4.5	4.0	–	–	MHz
			12	4.0	–	–	
Oscillator Frequency (-40°C to +85°C)		Osc_{in}	4.5	10.24	–	–	MHz
			12	10.24	–	–	

BLOCK DIAGRAMS



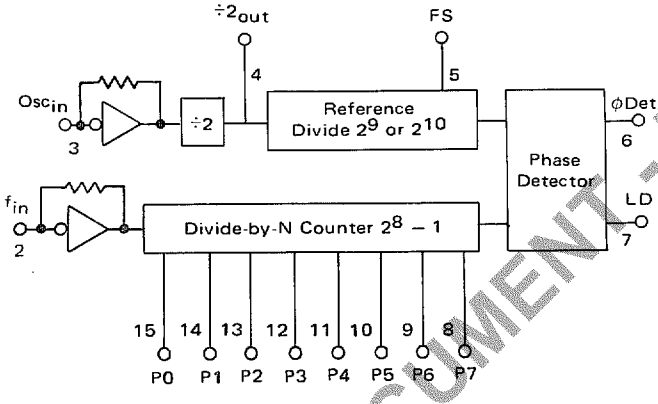
MC145104

V_{DD} = Pin 1
V_{SS} = Pin 16



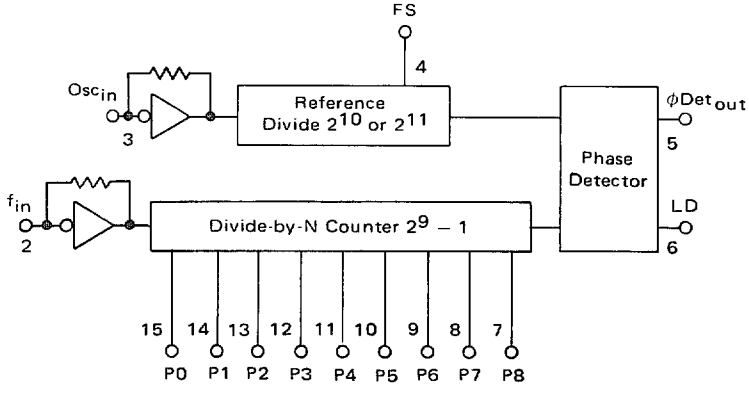
MC145106

V_{DD} = Pin 1
V_{SS} = Pin 18



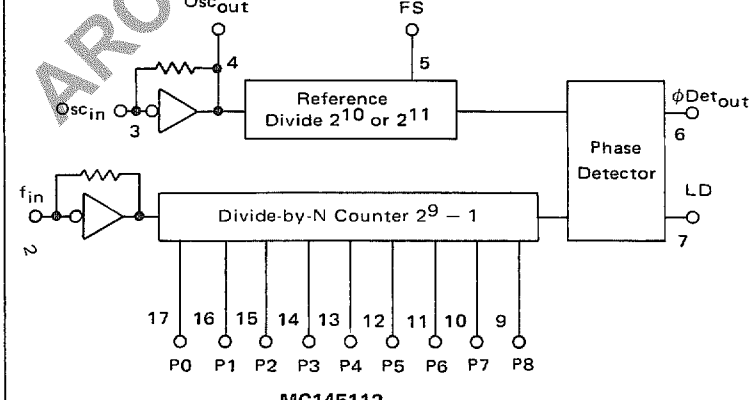
MC145107

V_{DD} = Pin 1
V_{SS} = Pin 16



MC145109

V_{DD} = Pin 1
V_{SS} = Pin 16



MC145112

N.C. = Pin 8
V_{DD} = Pin 1
V_{SS} = Pin 18

TYPICAL CHARACTERISTICS

FIGURE 1 – MAXIMUM DIVIDER INPUT FREQUENCY versus SUPPLY VOLTAGE

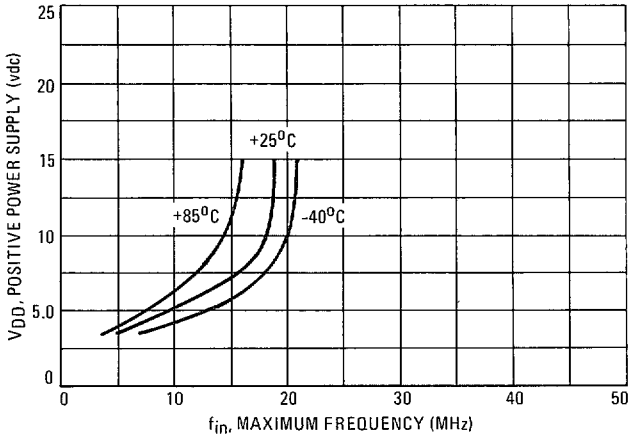
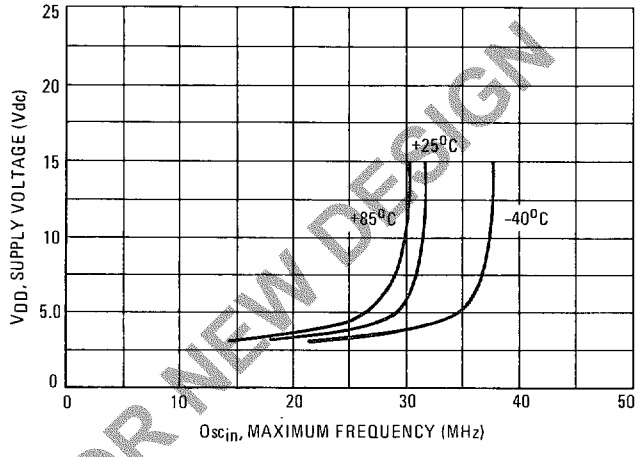


FIGURE 2 – MAXIMUM OSCILLATOR INPUT FREQUENCY versus SUPPLY VOLTAGE



TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide By N
0	0	0	0	0	0	0	0	0	2 (Note 1)
0	0	0	0	0	0	0	0	1	3 (Note 2)
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0	1	1	1	1	1	1	1	1	255
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}
0: Voltage level = 0 or open circuit input

Note 1: The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2^N-1 sequence. When pin is not connected (or is not listed as for the MC145104 and MC145107), the logic signal on that pin can be treated as a "0".

PIN DESCRIPTIONS

P0 – P8 – Programmable divider inputs (binary)
f_{in} – Frequency input to programmable divider (derived from VCO)
Osc_{in} – Oscillator/amplifier input terminal
Osc_{out} – Oscillator/amplifier output terminal
LD – Lock detector, low when out of lock
ϕ Det_{out} – Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator - input frequency typically 5.0 or 10 kHz.
FS – Reference Oscillator Frequency Division Select. When using 10.24 MHz Osc frequency, this control selects 10 kHz, a "0" selects 5.0 kHz.
$\div 2_{out}$ – Reference Osc frequency divided by 2 output; when using 10.24 MHz Osc frequency, this output is 5.12 MHz for frequency tripling applications.
V_{DD} – Positive power supply
V_{SS} – Ground

PLL SYNTHESIZER APPLICATIONS

The MC145104, MC145106, MC145107, MC145109, MC145112 ICs are well suited for Applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer using a single crystal reference is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145104-12 ICs can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling and loop programming techniques. In general, 300-400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft syntheizer of Figure 5, the VHF loop (top) will provide a 50 kHz 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal, 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720 channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on-frequency during transmit and is offset downward during receive. The offset corresponds to the receiver I F (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

FIGURE 3 – SINGLE CRYSTAL CB SYNTHESIZER FEATURING ON-FREQUENCY VCO DURING TRANSMIT

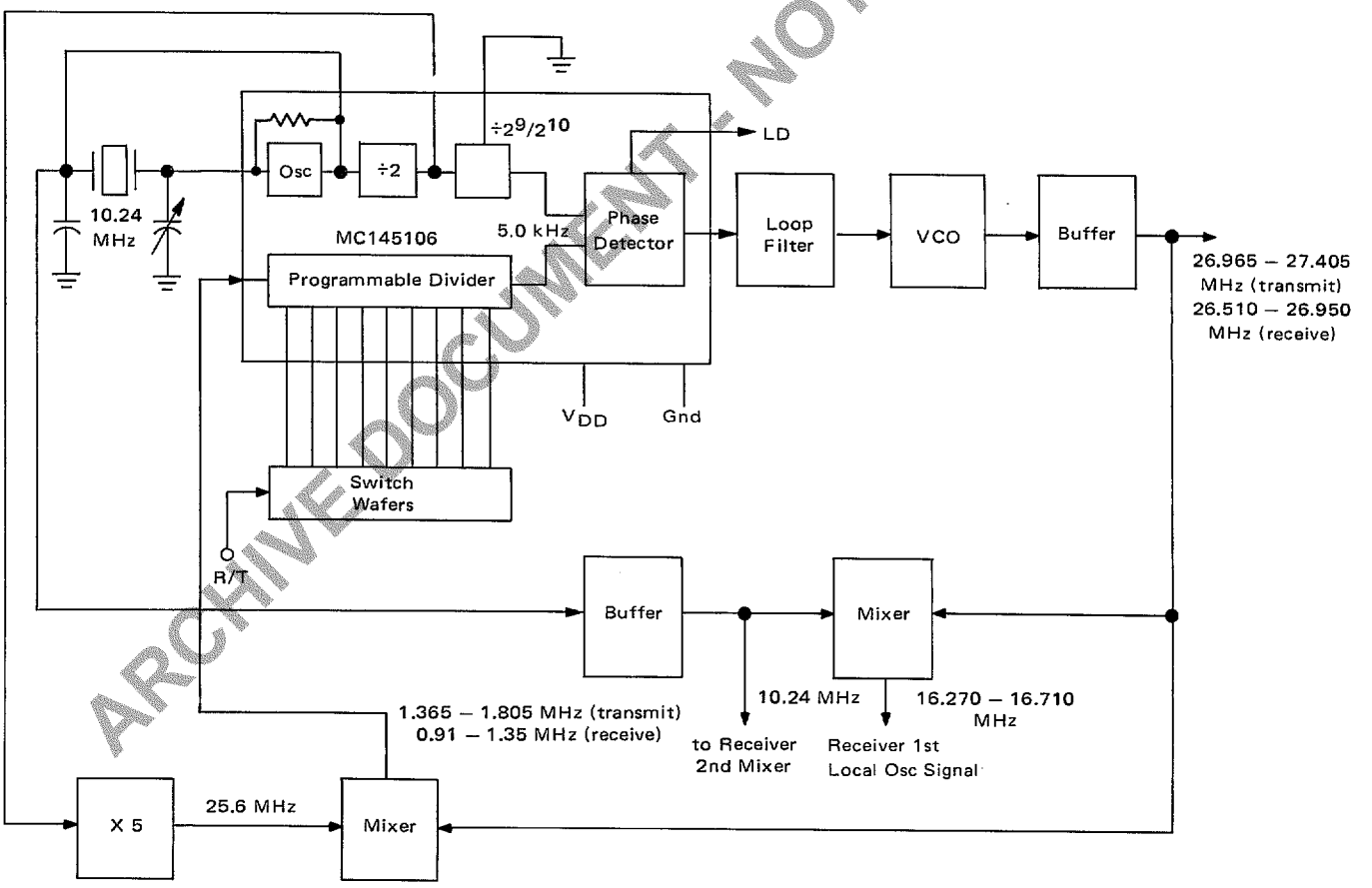
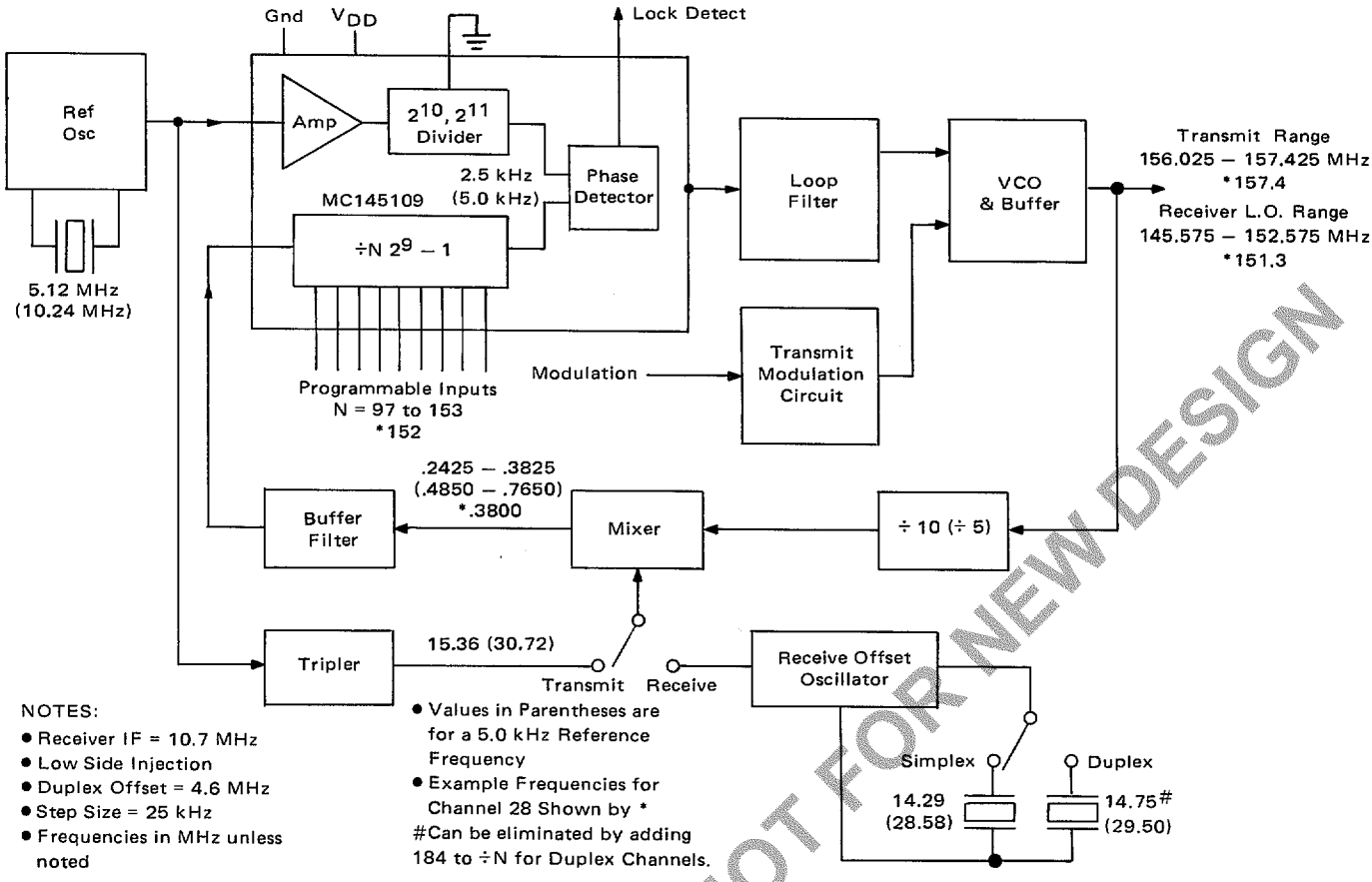


FIGURE 4 – VHF MARINE TRANSCEIVER SYNTHESIZER

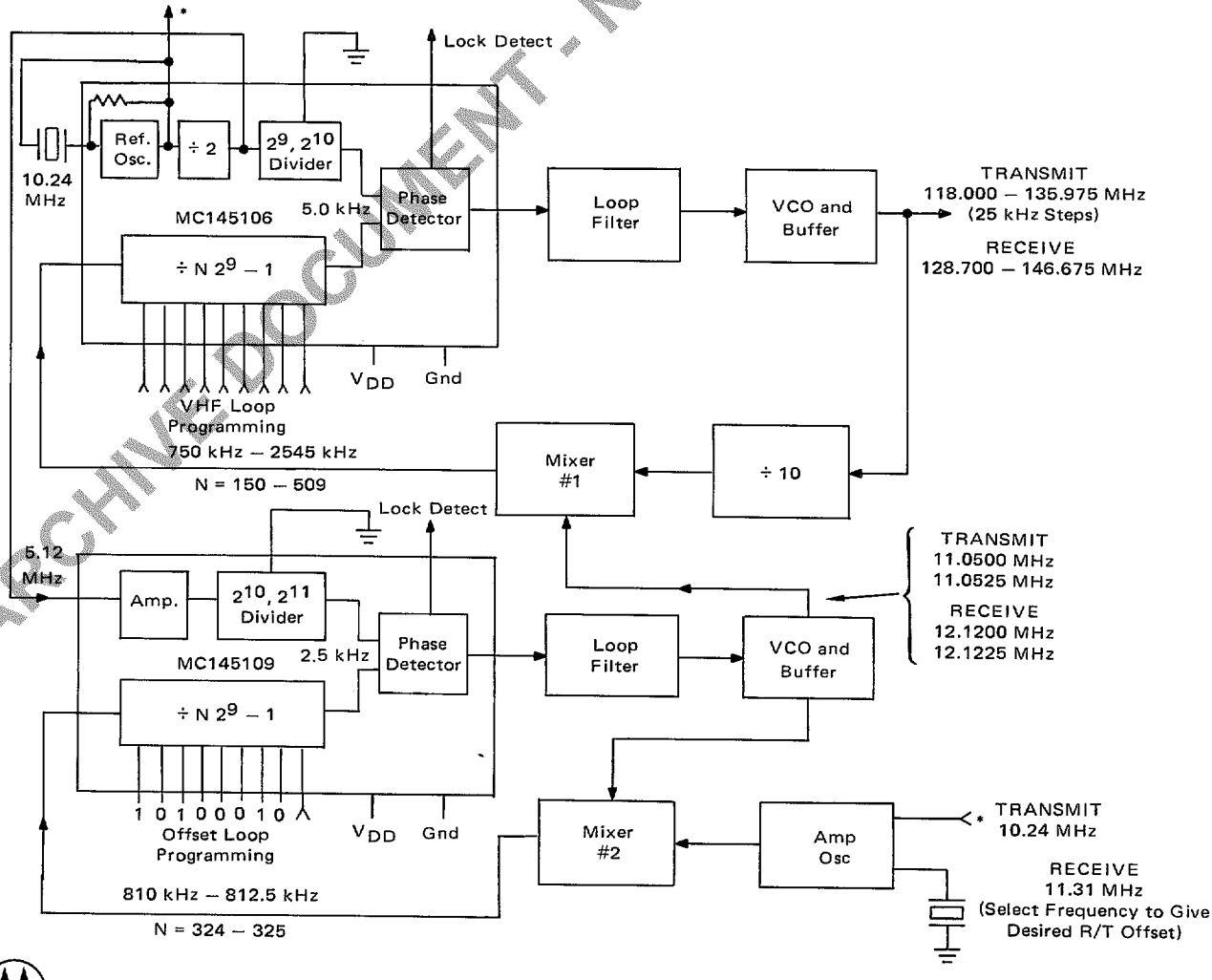


NOTES:
- Receiver IF = 10.7 MHz
- Low Side Injection
- Duplex Offset = 4.6 MHz
- Step Size = 25 kHz
- Frequencies in MHz unless noted

- Values in Parentheses are for a 5.0 kHz Reference Frequency
- Example Frequencies for Channel 28 Shown by *

#Can be eliminated by adding 184 to ÷N for Duplex Channels.

FIGURE 5 – VHF AIRCRAFT 720 CHANNEL TWO CRYSTAL FREQUENCY SYNTHESIZER



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