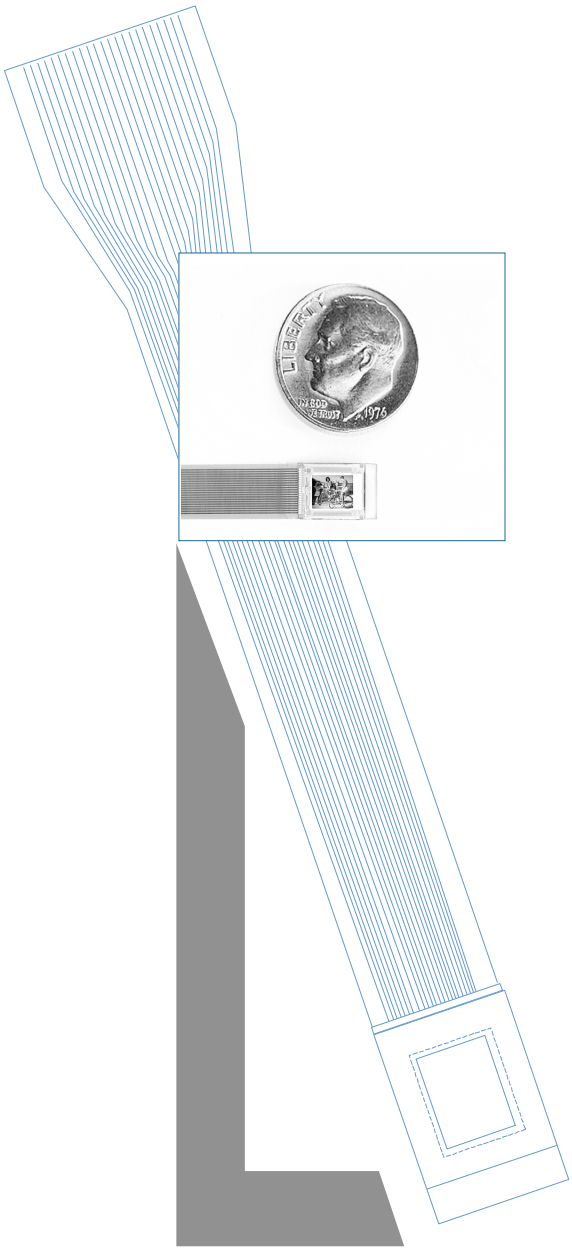
KOPIN

CyberDisplay™



CyberDisplay™ 320 Monochrome Display Model 290 KCD-QD01-BA

Specifications

For Use With RS170 Module

Kopin Corporation

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2/22/2001 KLQS-007-A-B

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1. Electrical Specifications

The CyberDisplay 320 is an active-matrix liquid crystal display, with 320 × 240 spatial resolution with a high efficiency Cyberlite™ backlight. The display is fabricated in a high speed, low power CMOS process utilizing single crystal silicon-on-insulator (SOI) starting material. The display's integrated horizontal and vertical shift registers with thin film transistors meet the performance demands of high-speed video applications. The display uses complementary analog video inputs. All digital control inputs accept 3.3 - 5.0 -volt levels.

1.1 Features

- 320 (H) × 240 (V) spatial resolution (76,800 pixels).
- Active pixels 290 × 218 (63,200 pixels).
- 3.3 - 5.0 volt CMOS logic compatible control signals with built-in level-shifter
- Low power consumption - 12mW
- High performance - up to 72 frames per second
- 1 positive and 1 negative polarity staggered analog video inputs
- Integrated horizontal and vertical shift registers
- Ultra-compact size - Active display area 4.8 mm x 3.6 mm (0.24 inches diagonally)

The display products and systems described herein are covered by numerous issued U.S. and foreign patents and pending applications owned by or licensed to Kopin Corporation.

1.2 AMLCD Specifications

Figure 1-1. CyberDisplay 320 Block Diagram

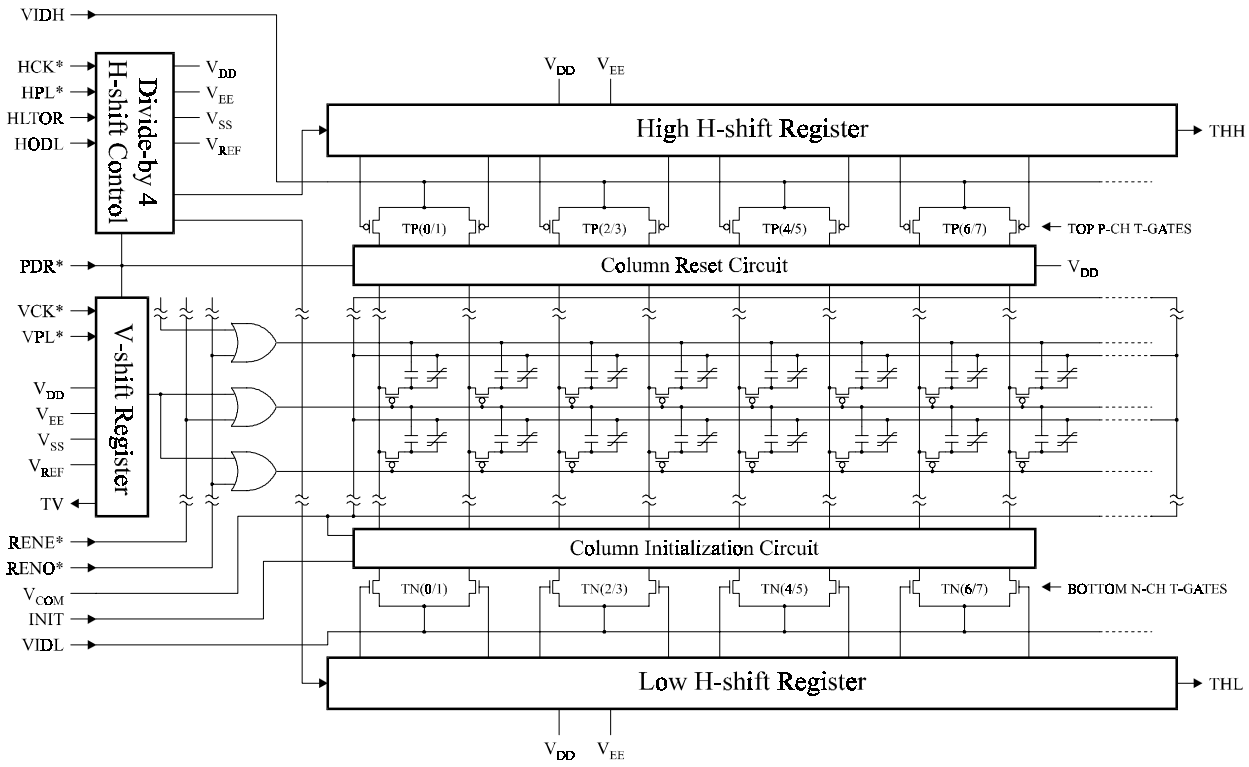


Table 1-1. Absolute Maximum Ratings

Parameter/Condition	Symbol	Rated Value	Units
Supply Voltage - Source	V_{DD}	-0.5 to +12	V
Supply Voltage - Sink	V_{EE}	V_{DD} - 11 (≥ -0.5) to V_{DD} + 0.5	V
High Video Signal	VIDH	-0.5 to V_{DD} + 0.5	V
Low Video Signal	VIDL	-0.5 to V_{DD} + 0.5	V
All Inputs	V_I	-0.5 to V_{DD} + 0.5	V

Note

Permanent damage to the display may result if Absolute Maximum Ratings in the above table are exceeded. The Absolute Maximum Ratings are not typical operating conditions.

Table 1-2. Electrical Characteristics and Recommended DC Operating Conditions

(Notes: 1, 2, 3) (V_{DD}= 9V ± 0.5V, V_{EE}= 2V ± 0.2V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage - Source	V_{DD}	8.5	9.0	9.5	V
Supply Voltage - Sink	V_{EE}	1.8	2.0	2.2	V
Operating Current: Power Supply - Source	I_{VDD}		1.6	2.6	mA
Operating Current: Power Supply - Sink	I_{VEE}		-1.0	-1.7	mA
Operating Current: GND	I_{VSS}			-0.9	mA
Video Signal Center Voltage	V_{VC}		$(V_{DD} + V_{EE})/2$		V
Video Common Voltage	V_{COM}		V_{VC} + 0.4		V
Video Common Current	I_{VCOM}			10	µA
High Video Voltage (VIDH)	V_{VIDH}	V_{VC} (Wht)		V_{DD} (Blk)	V
Low Video Voltage (VIDL)	V_{VIDL}	V_{EE} (Blk)		V_{VC} (Wht)	V
Input Reference Voltage	V_{REF} (3.3V Logic)	1.7	1.8	1.9	V
	V_{REF} (5.0 V Logic)	2.2	2.3	2.4	V
Input Reference Current	I_{VREF} (3.3V Logic)			10	µA
	I_{VREF} (5.0V Logic)			10	µA
Input High Voltage, excluding PDR*	V_{IH} (3.3V Logic)	2.9			V
(See note 8)	V_{IH} (5.0V Logic)	4.4			V
Input Low Voltage, excluding PDR*	V_{IL} (3.3V Logic)			0.3	V
(See note 8)	V_{IL} (5.0V Logic)			0.5	V
Input High Voltage, PDR* (See note 9)	V_{IHPDR}	3.3			V
Input Low Voltage, PDR* (See note 9)	V_{ILPDR}			0.5	V
Input Current	I_{IPDR}			10	µA

Table 1-3. Capacitance

Parameter	Symbol	Min.	Typ.	Max.	Units
Input Capacitance: HPL*, VPL*, HCK*, VCK*, PDR* RENE*, RENO*, HODL, HLTOR	C_C			10	pF
Input Capacitance: VREF	C_{VREF}			40	pF
Input Capacitance: VCOM	C_{VCOM}			300	pF
Input Capacitance: VIDH, VIDL	C_V	40	50	60	pF

Table 1-4. Display Power Consumption

Parameter	Symbol	Min.	Typ.	Max.	Units
Power consumption of the display	PWR		12.0	22.0	mW

Table 1-5. Electrical Characteristics and Recommended AC Operating Conditions

(Notes: 4,5,6) (V_{DD}= 9V ± 0.5V, V_{EE}= 2V ± 0.2V)

Parameter	Symbol	Min.	Typ.	Max.	Units
VCK* period	t_{VC}	101.4			µs
VCK* high pulse width	t_{VCH}	290			ns
VCK* low pulse width	t_{VCL}	290			ns
VPL* setup time	t_{VPS}	140			ns
VPL* hold time	t_{VPH}	140			ns
VCK* to RENE*/RENO* delay time	t_{VCRD}	440			ns
RENE*/RENO* to VCK* delay time	t_{VRCD}	440			ns
RENE*/RENO* to RENO*/RENE* delay time	t_{VRED}	890			ns
HODL to HCK* time	t_{HOH}			40	ns
HCK* period	t_{HC}	150			ns
HCK* high pulse width	t_{HCH}	65			ns
HCK* low pulse width	t_{HCL}	65			ns
HPL* setup time	t_{HPS}	60			ns
HPL* hold time	t_{HPH}	40			ns
Transition time (rise or fall)	t_{T}	3		10	ns
HCK* to video setup time	t_{HVS}			70	ns
HCK* to video hold time	t_{HVH}	190			ns
Video delay time	t_{VD}	890			ns
Video lead time	t_{VL}	890			ns
RENE*/RENO* power down pulse width	t_{VRP}	6.0			µs

Notes

1. All voltages referenced to V_{SS}.
2. I_{VDD}, I_{VEE}, I_{VSS}, and PWR are dependent on operating frequency.
3. Values are obtained with display operating at 72 frames per second.
4. AC characteristics assume ^{t}T = 3 ns. Transition times are measured between V_{IH} (MIN) and V_{IL} (MAX), or between V_{IL} (MAX) and V_{IH} (MIN). All control signals must transit in a monotonic manner.
5. Alternation of HODLs logic state for every row plus alternation at row 0 of successive frames is required to support the pixel inversion driving scheme (see Figure 2-4). Alternation of HODL's logic state between successive frames is required to support the column inversion driving scheme (see Figure 2-3).
6. A power-down cycle is required before power to display is removed. After PDR* has been asserted, either a 1 RENE* and 2 RENO*, or a 2 RENE* and 1 RENO* pulse sequence is required for completion of the cycle.
7. The ''*'' symbol indicates signal is active low.
8. Parameters for signals HCK*, HPL*, VCK*, VPL*, RENE*, RENO*, HODL, HLTOR.
9. Parameters For signal PDR.

Figure 1-2. Vertical Timing

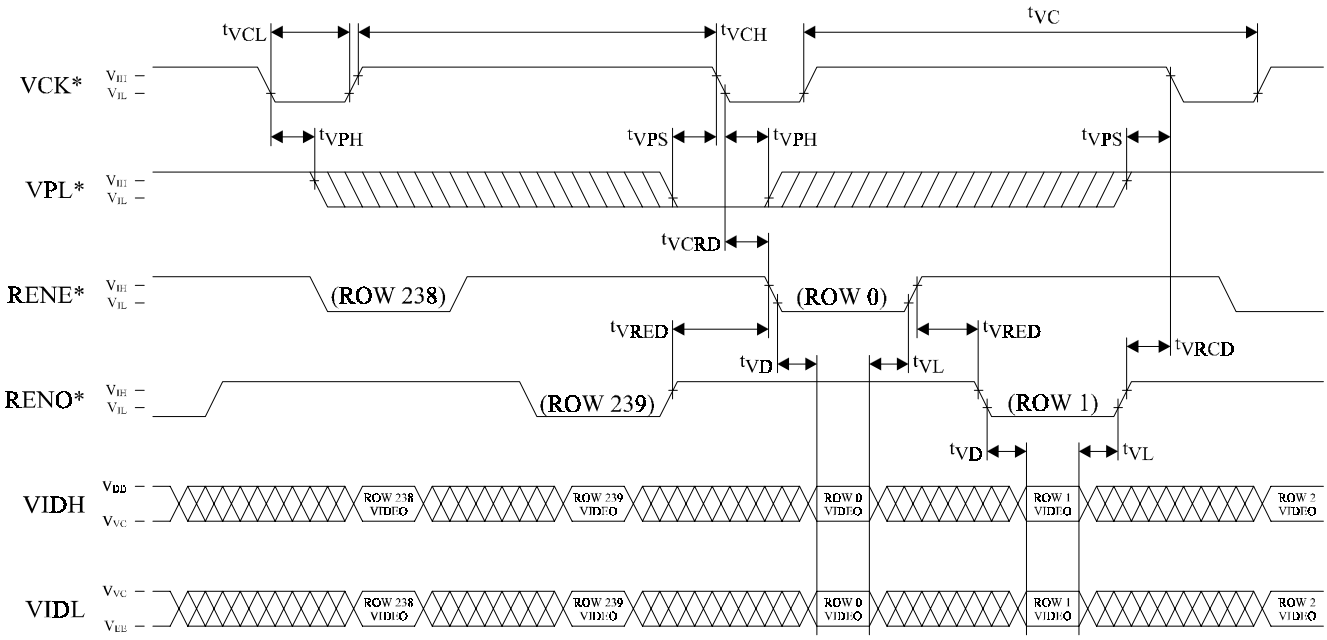
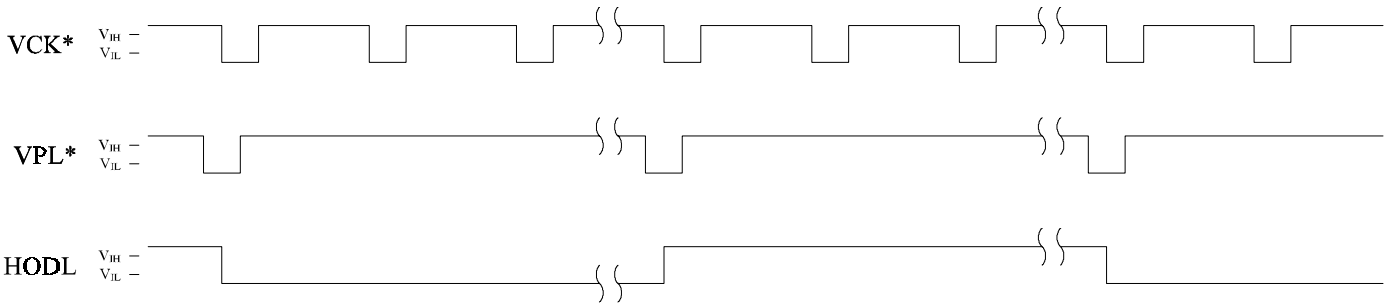


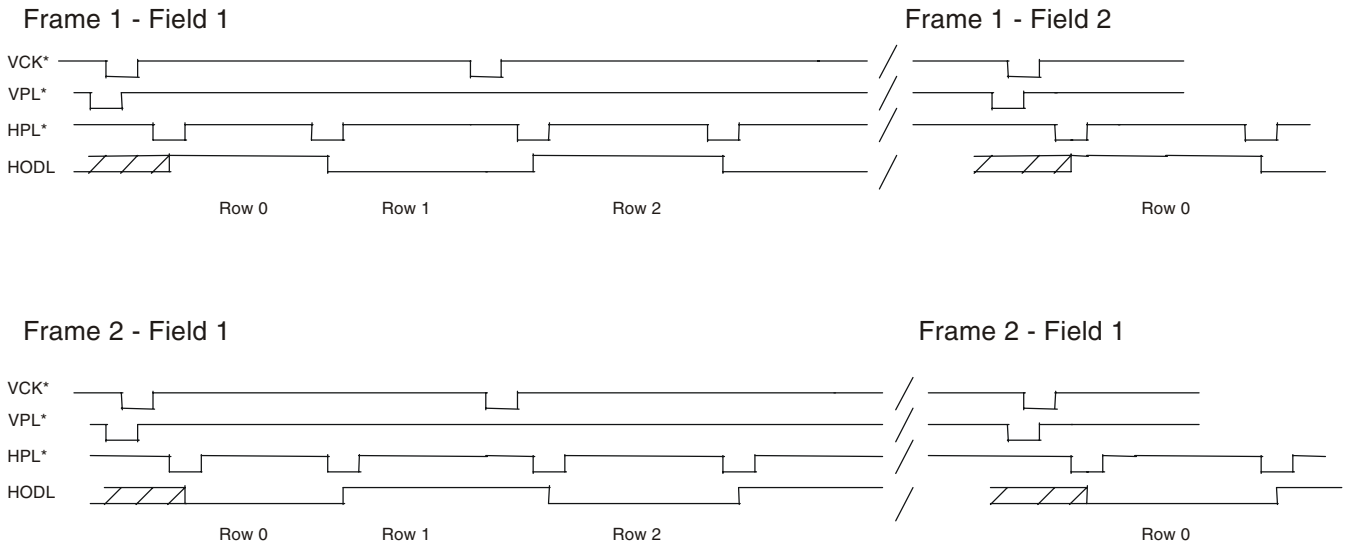
Figure 1-3. Column Inversion Timing



Note

HODL's logic state must be altered between successive frames to support the column inversion driving scheme.

Figure 1-4. Pixel Inversion Timing



Note

HODL must toggle every row, additionally the phasing shall toggle every frame. At row 0 of frame 1 of field 1 and 2, HODL is at high level and toggles every row thereafter. At row 0 of frame 2 of field 1 and 2 HODL is at low level and toggles every row thereafter.

Figure 1-5. Horizontal Timing

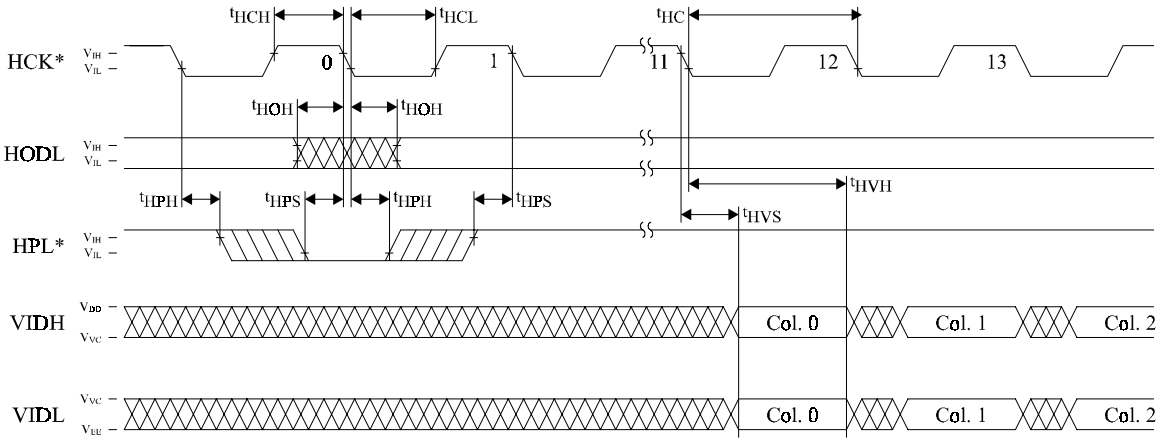
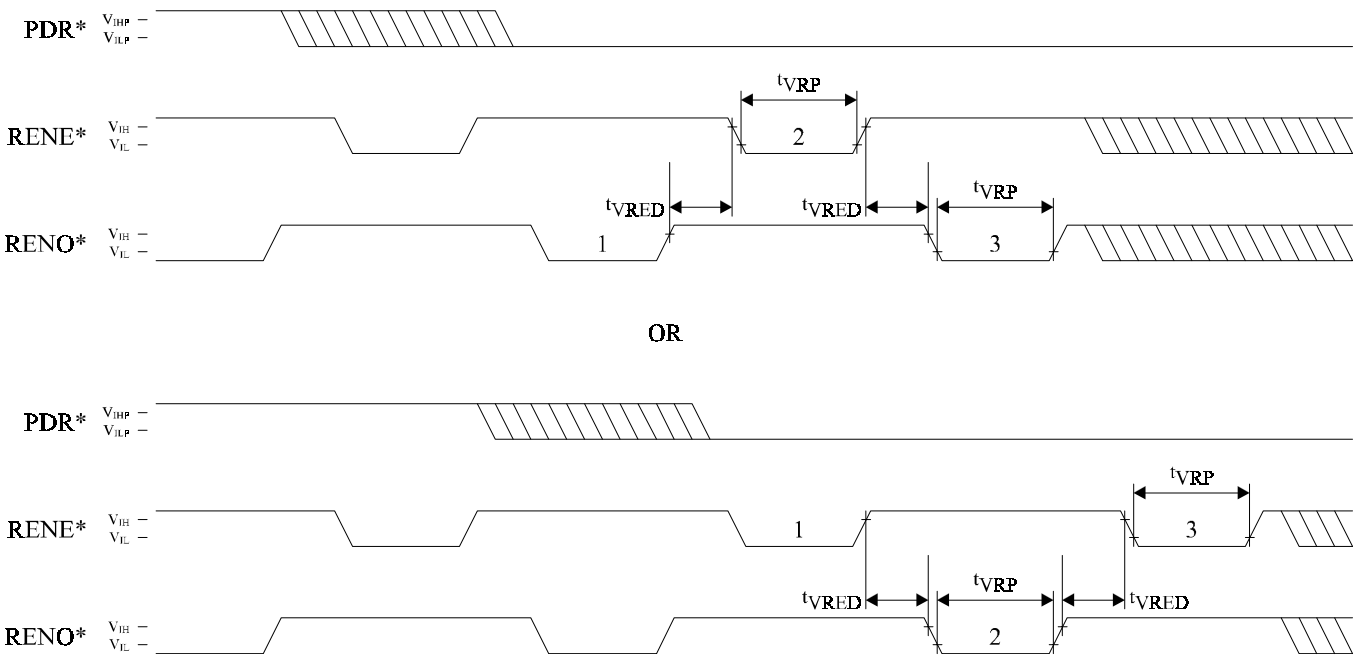


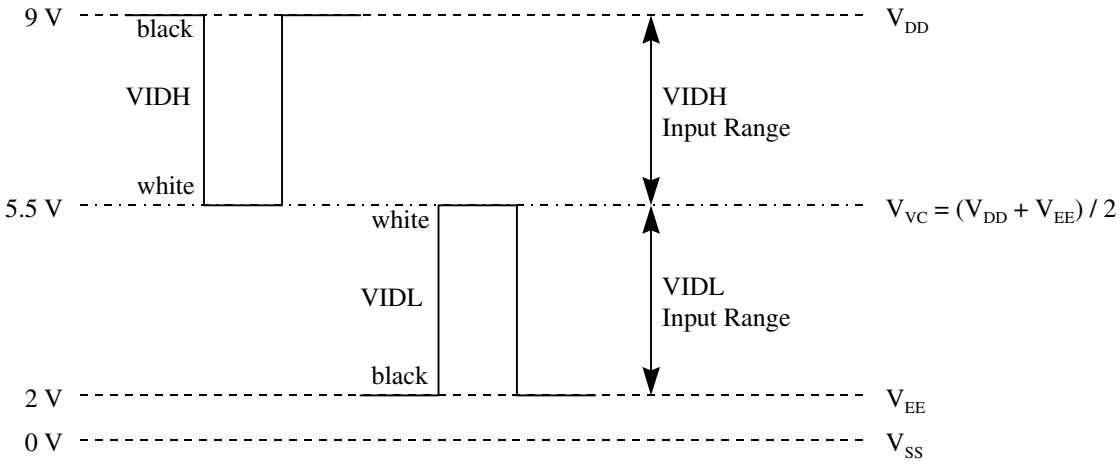
Figure 1-6. Power Down Cycle Timing



Note

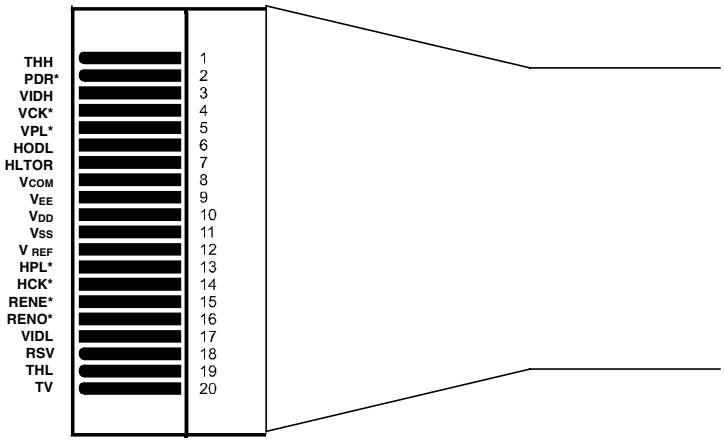
A power-down cycle is required before power to display is removed. After PDR* has been asserted, either a 1 RENE* and 2 RENO*, or a 2 RENE* and 1 RENO* pulse sequence is required for the completion of the power-down cycle.

Figure 1-7. Typical Operating Voltages



1.3 Pinout Assignment

Figure 1-8. Pin Assignment Flex End



View through circuit flex. Contacts exposed on far side

Table 1-6. Pinout Assignment

Pin No.	Symbol	Description
1	THH	Test pin. High H-shift register output
2	PDR*	Power Down Reset. Asserted low during power-down cycle
3	VIDH	High (positive polarity) video signal
4	VCK*	Vertical clock , V-shift register
5	VPL*	Vertical start pulse, V-shift register
6	HODL	Horizontal odd low. Asserted high for odd columns to receive low video input
7	HLTOR	Horizontal left to right. Asserted high for left-to-right scan
8	V_{COM}	Common voltage
9	V_{EE}	Supply voltage - Sink
10	V_{DD}	Supply voltage - Source
11	V_{SS}	GND
12	V_{REF}	Input level reference voltage
13	HPL*	Horizontal start pulse, H-shift register
14	HCK*	Horizontal clock, H-shift register
15	RENE*	Even rows enable
16	RENO*	Odd rows enable
17	VIDL	Low (negative polarity) video signal
18	RSV	Test pin. Must be grounded for proper operation of display
19	THL	Test pin. Low H-shift register output
20	TV	Test pin. V-shift register output

The * Symbol indicates signal is active low

Note **Pin 18 (RSV) must be tied to ground for proper operation of the display.**

2. Optical Characteristics

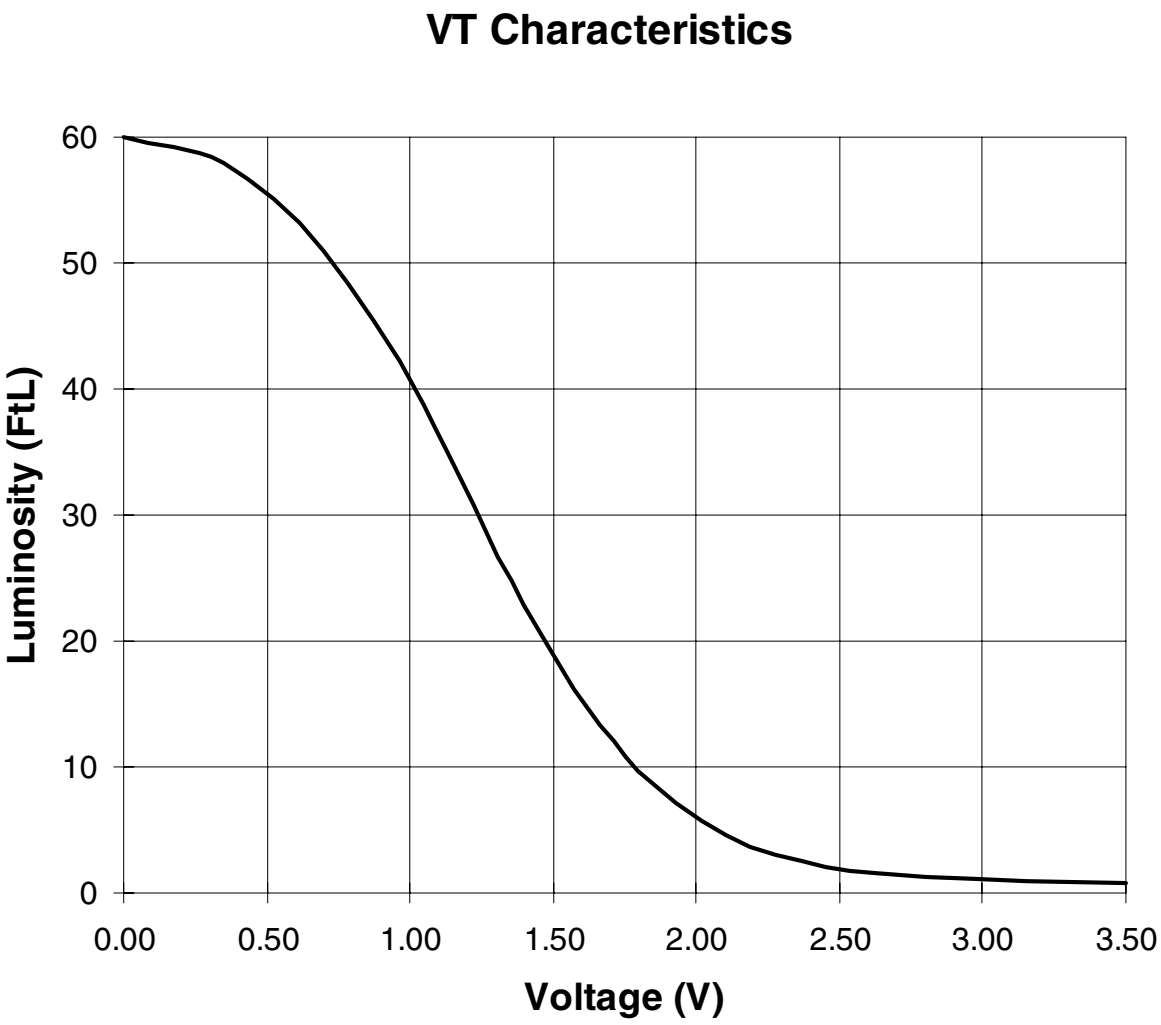
Table 2-7. Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Contrast Ratio		CR_{25}	1	60	90	-	_
Optical Transmittance		T	2	5.5	7.0	-	%
VT Characteristics	V90	$V_{90\ 25}$	3	0.25	0.50	0.75	V
	V50	$V_{50\ 25}$		0.50	1.00	1.50	
	V10	$V_{10\ 25}$		1.20	1.70	2.20	
Response Time	Ton	$T_{on\ -25}$	4	-	15	20	
	Toff	$T_{off\ 25}$		-	50	80	
Flicker		F_{25}	5	-	-	-40	dB
Image Retention Time		IRT	6	-	-	60	sec
Transmission Uniformity		TU	7	-	0.5%	1.5%	delta
Chromatic Uniformity		CU	8,9		0.002	0.010	radius
Color Gain		CG	10		2000	2500	K

Condition

1. Ratio of white image/black image.
2. Based on 1 degree aperture.
3. Vrms
4. 10% to 90% transmission.
5. 20log (AC/DC) @50% transmission, 25Hz HODL.
6. Decays to less than 1% full grey scale.
7. 5 point uniformity of unpowered display (maximum deviation from center).
8. Deviation, relative to center, of color from 5 point uniformity measurement.
9. Deviation specified as radius, about the color of the center of the display in (u', v') colors.
10. Measured at the center of unpowered display. Backlight: 7300K

Figure 2-1. VT Characteristics



3. Display Mechanical Specifications

The CyberDisplay™ 320 display is factory sealed into a polycarbonate module. This module performs the following important functions:

- Seals the display from the environment.
- Contains and protects the two polarizing elements.
- Provides robust strain relief for flex PC cable.
- Provides visual framing of the display aperture.
- Masks extraneous light from the backlight.
- Provides mechanical interface with precise registration.

The CyberDisplay 320 Display Module is designed for snap assembly to Kopin CyberLite™ backlight module. Customers providing their own backlights can register to the features provided on the display module. Four notches in the viewing face are intended to interface with snap features on the backlight.

The flexible PC cable is strain relieved, but tugging forces should be limited to less than 1 lb. in any direction. The minimum inside bend radius for the cable is .03 inches. Repeated reformings are not recommended.

Figure 3-1. CyberDisplay™ 320 Display Dimensions Viewing Side

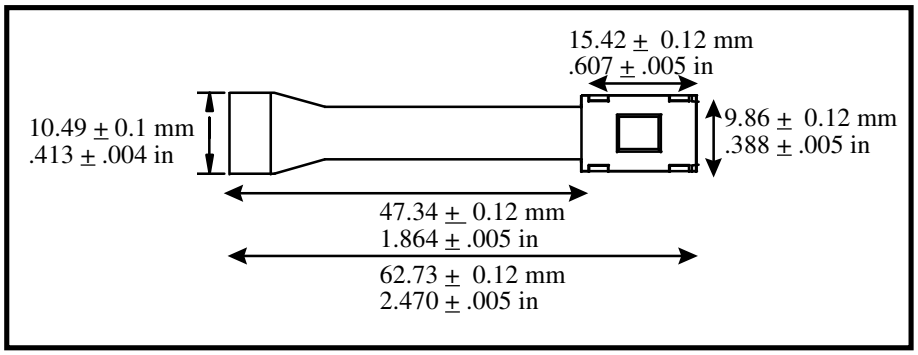


Figure 3-2. CyberDisplay™ 320 Display Dimensions Side View

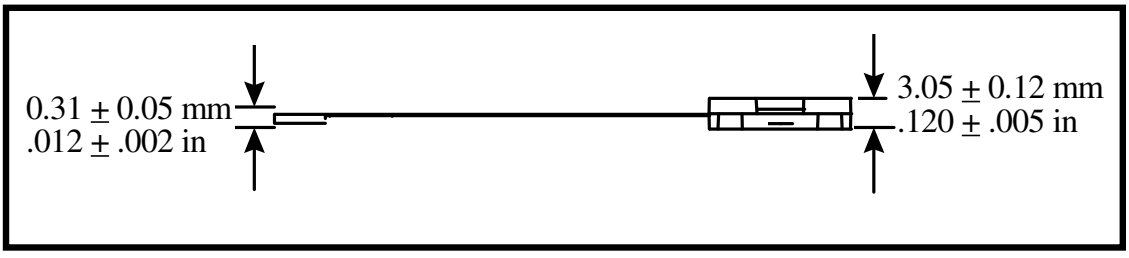


Figure 3-3. CyberDisplay™ 320 Display Dimensions Viewing Area

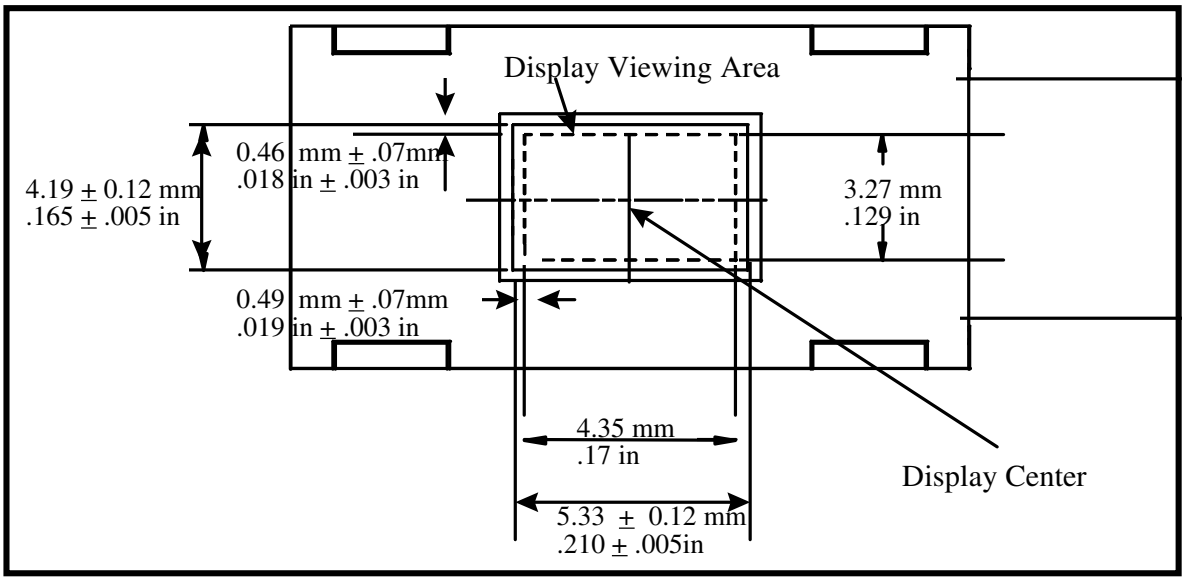


Figure 3-4. Display Interconnect Specification

Display Interconnect	Flex PC, 1.86in free length, 20 conductor, 0.5mm pitch to mate with JST 20FLZ-RSM1-TB, Hirose FH12-20S-0.5SH, Molex AE-52892-2090, Molex AE-52746-2090, or equivalent connector.

4. Environmental Specifications

Table 4-8. CyberDisplay™ 320 Display Environmental Specifications

Storage Temperature	-20°C to 80°C
Operating Temperature	-20°C to 60°C
Humidity, Storage and Operating	40°C at 80% humidity for 240 hours operating at 25Hz HODL.
Shock	4 foot drop to concrete
Vibration	20 to 2,000 hz, 6G's RMS maximum 3 axes, 10 minutes each axis
ESD - Human Body Model	2500V Electrical Discharge

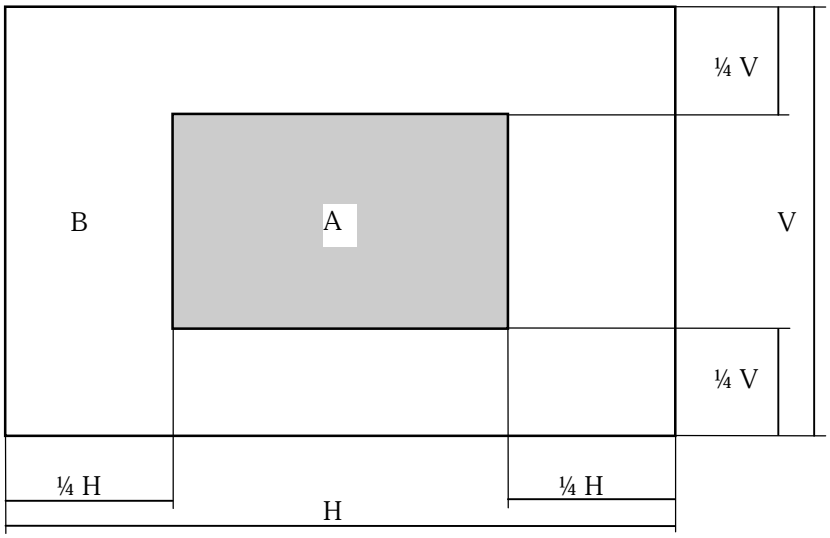
5. Display Appearance Specification

Table 5-1. Display Appearance

Defect Type	**Defect Criteria**	
Circuit	No partial or faded image, no streaking or shadow, no unstable image.	
Line	Not allowed	
Pixel	See Figure below	
Adjacent pixels	Two or more.	Same criteria as for pixel defects, based on aggregate brightness (See figure below).
Polarizer	Brightness: Size:	Same criteria as for pixel defects (see figure below). Diffuse, out of focus blemishes are allowed.

Test Conditions: Test board runs in pixel inversion at 30 Hz HODL rate (NTSC) or 25 Hz (PAL).
Limit Samples: Reference limit samples will be used for pixel and polarizer defect types.

Figure 5-1. Display Appearance Specification



ZONE	DEFECT	NUMBER
A	S or M	1
	L	0
B	S or M	3
	L	1

where:

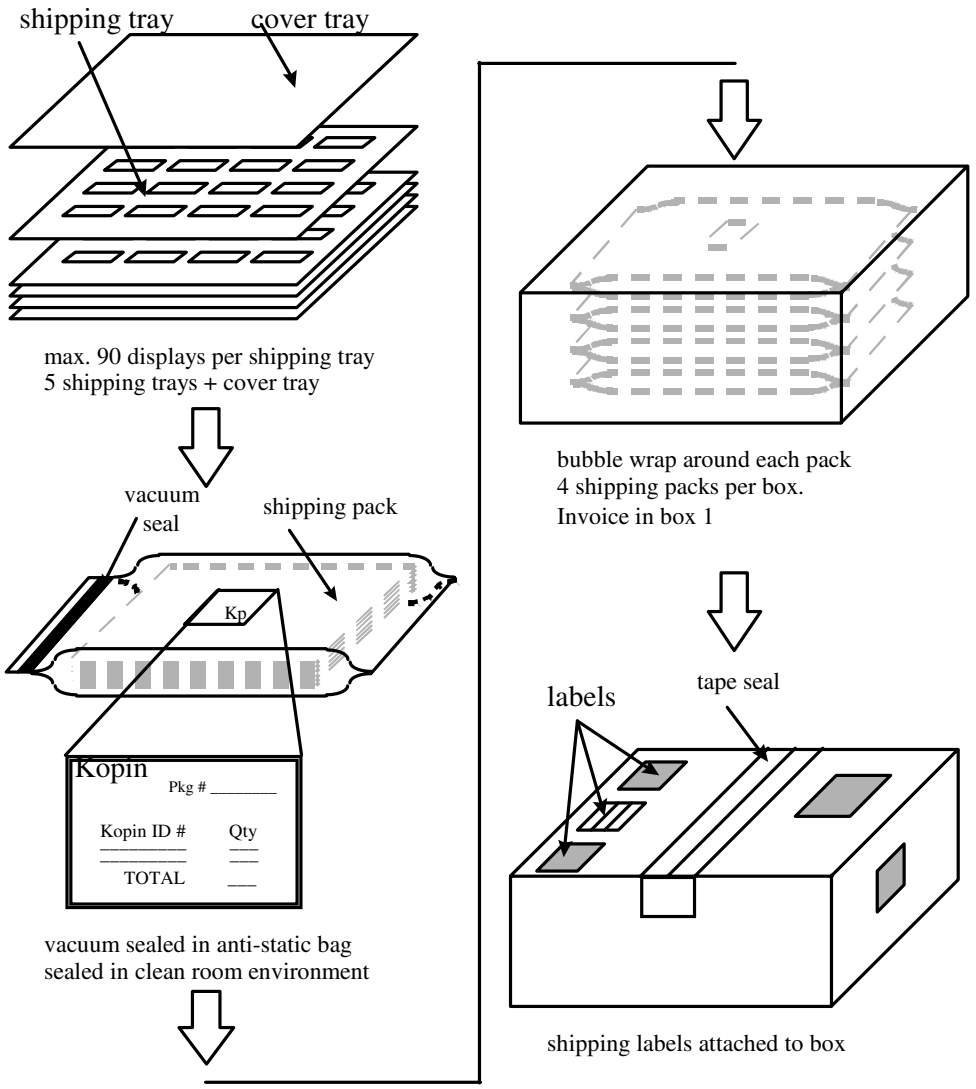
Small (S) defect differs from nominal pixel brightness by 10 - 25%.
Medium (M) defect differs from nominal pixel brightness by 25 - 75%.
Large (L) defect differs from nominal pixel brightness by ≥ 75%.
Defect can be black or white spot.

6. Packaging and Handling Information

6.1 Display Panel Shipping Package

Display panels are packaged in an antistatic tray approximately 12 inches by 15 inches. The tray holds 90 displays. The trays stack on top of each other, with the bottom of one tray being the top of the one underneath. The trays are stacked 5 deep and an empty tray placed on top of the stack. The stack of trays is vacuum sealed in a moisture barrier metallic bag. A fully populated bag contains 450 displays and is approximately 2.5 inches high. Each bag has an identification sticker attached for tracability. An electrostatic sensitive devices label is also affixed to the outside of the antistatic bag. The packaging of trays and sealing is done in a class 10 clean room environment. See Figure below.

Figure 6-1. Display Panel Shipping Package



Four bags of displays are placed in a shipping carton giving a total of 1800 displays in a fully populated shipping carton. The bags are wrapped with bubble wrap for protection during shipping. The appropriate shipping documentation is affixed to the carton.

6.2 Handling the Display

The display bag should be opened in a clean environment, preferably in an assembly area. Normal electrostatic precautions should be followed when handling the displays. The stack of display trays will be loosely held together when removed from the bag. Once taken from the bag, the stack of trays should be held from the bottom to provide support when moving. To open the bag, place the display bag on a flat surface with the label side up. Using a blade or knife carefully trace along two adjacent edges of the bag to cut open the bag. Slide the stack of trays out of the bag.

Normal electrostatic precautions should be followed when handling the displays and assembling the display and backlight. The displays should be assembled in a clean environment so as to minimize the possibility of dust particles being deposited on the display viewing area. A class 10,000 or better clean room environment is recommended. Vinyl anti-static gloves or static-dissipative finger cots should be used when assembling the display and backlight module. The preferred method for removing displays from the tray is to use a vacuum pen or tweezers and grasp the display at the middle of the flex cable.